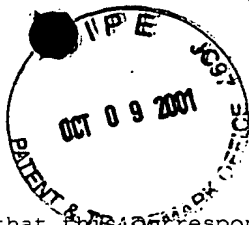


GR 99 P 1058



*Aug 10/01*

2819

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

By:

*Loren D. Pearson*

Date:

*10/2/01*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Wilfried Daehn

Appl. No. : 09/484,781

Filed : January 18, 2000

Title : Integrated Semiconductor Circuit and Method  
for Functional Testing of Pad Cells

Examiner : Don Le

Group Art Unit : 2819

A M E N D M E N T

Hon. Commissioner of Patents and Trademarks  
Washington, DC 20231

S i r :

Responsive to the Office action dated July 2, 2001, kindly  
amend the above-identified application as follows:

In the Claims:

Cancel claim 4.

*A*  
Claim 1 (amended). An integrated semiconductor circuit,  
comprising: